are traversed, and reconsideration and withdrawal thereof respectfully requested. The following is a comparison between the invention as claimed and the cited prior art.

An aspect of the invention, per claim 13, is a method of manufacturing an integrated semiconductor device having a plurality of semiconductor elements formed in a semiconductor layer. Each semiconductor element has a source of a first-conductivity-type semiconductor, a drain of the first-conductivity-type semiconductor and a body region of a second-conductivity-type semiconductor between said source and said drain. The method comprises the steps of implanting impurities concurrently into at least a predetermined part of the drain of one semiconductor element and into a predetermined part of the drain of another semiconductor element. An implantation mask is used that includes a portion corresponding to the drain of the one semiconductor element and has a first opening ratio as well as a portion corresponding to the drain of the another semiconductor element and has a second opening ratio different from the first opening ratio. The one semiconductor element has a breakdown voltage higher than that of the another semiconductor element. The implantation mask used has the first opening ratio smaller than the second opening ratio. The one semiconductor element is adjacent to the another semiconductor element. A wall-shaped element-isolation insulating film for isolating the one semiconductor element from the another semiconductor element is provided in the semiconductor layer prior to the step of implanting impurities. The integrated semiconductor device is annealed after the step of implanting impurities to diffuse the impurities.

The Examiner asserted that Hayashi (Figs. 1-4) discloses a method of manufacturing an integrated semiconductor device formed in a semiconductor layer having sources and drains, and implanting impurities through an implantation mask having different opening ratios (A, A'). The Examiner further asserted that Hayashi discloses that the semiconductor elements have different

breakdown voltages. The Examiner acknowledged that Hayashi lacked anticipation of a wall-shaped element isolation insulating film for isolating one semiconductor element from another semiconductor element prior to the step of implanting impurities.

The Examiner averred that Minato (para. [0113] and Figs. 100-116) discloses a method of manufacturing an integrated semiconductor device formed in a semiconductor layer having sources 6 and drains 3 of a first conductivity type and a body region 5 of a second conductivity type between said source and drain, and providing a wall-shaped element-isolation film 23 for isolating one semiconductor element from another semiconductor element prior to the step of implanting impurities. The Examiner further asserted that Hayashi (Fig. 4) and Minato (para. [0396] and [0404]) disclose that the masks include stripe-shaped masks. The Examiner concluded that one of ordinary skill in the art would have been motivated to incorporate wall-shaped element-isolation films to ensure isolation of the semiconductor elements.

Hayashi and Minato do not suggest the claimed method of manufacturing an integrated semiconductor device because it would not have been obvious to one of ordinary skill in this art. Minato et al. is directed towards forming twin trench semiconductor devices comprising steps of forming trenches and implanting dopant into the trench sidewalls. Hayashi, on the other hand, is directed to a very different process of forming a semiconductor device. One of ordinary skill in this art would not look to the non-analogous process of forming semiconductor devices of Minato to seek improvements to the Hayashi process.

It would further not be obvious to combine Minato with Hayashi as asserted by the Examiner because Minato discloses many different embodiments of manufacturing a semiconductor device. The Examiner picks and chooses among the many different embodiments to reconstruct the claimed method using hindsight. There is no motivation to combine the

different embodiments of Minato as done by the Examiner. A reference must clearly and unequivocally disclose the claimed invention "without any need for picking, choosing, and combining various disclosures not directly related to each other by the teachings of the cited reference." *In re Arkley*, 455 F.2d 586, 587, 172 USPQ 524 (C.C.P.A. 1972).

According to the present invention a plurality of different mask openings ratios are used to perform the step of implanting impurities into drains, the impurities are made uniform in the subsequent step of diffusing the impurities, and therefore, semiconductor elements can have respective portions of the drains that are different in impurity concentration from each other. In addition, the present invention includes the step of providing a wall-shaped isolation region between the semiconductor elements to isolate the semiconductor elements from each other, thereby preventing impurities in a semiconductor element from diffusing into another semiconductor element.

In contrast thereto, the trench employed by Minato is used as a passage for directing impurities into the silicon substrate, not for isolating a semiconductor element from another semiconductor element. Therefore, the trench of Minato cannot ensure the isolation of a semiconductor element from another semiconductor element, as required by claim 13.

The present invention is further distinguishable over Minato because the regions separated from each other by the trench in Minato belong to the same semiconductor device. Thus, Minato's regions are not respective components of different semiconductor elements, as required by claim 13. Further Minato employs the step, immediately after the step of forming trenches, of forming a p-type layer and an n-type layer in each of the regions separated by trenches. Therefore, if the diffusion step of the present invention is applied to Minato to make impurities uniform, a transistor cannot be produced in the structure of Minato.

In addition to the method of the present invention and the Minato method being very different from each other, the object of the Minato invention is to improve the withstand (breakdown) voltage of one transistor, while an object of the present invention, which includes a plurality of transistors, is to simultaneously improve the on resistance and breakdown voltage of each of the transistors. Due to the vast differences between the cited references and the present invention, the present invention cannot be arrived at even if the methods of Hayashi are combined with the methods of Minato.

Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge readily available to one of ordinary skill in the art. *In re Kotzab*, 217 F.3d 1365, 1370 55 USPQ2d 1313, 1317 (Fed. Cir. 2000); *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992); *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). There is no suggestion in Minato to modify Hayashi as alleged by the Examiner to arrive at the invention of claim 13.

The requisite motivation to support the ultimate legal conclusion of obviousness under 35 U.S.C. § 103 is not an abstract concept, but must stem from the applied prior art as a whole and realistically impel one having ordinary skill in the art to modify a specific reference in a specific manner to arrive at a specifically claimed invention. *In re Deuel*, 51 F.3d 1552, 34 USPQ2d 1210 (Fed. Cir. 1995); *In re Newell*, 891 F.2d 899, 13 USPQ2d 1248 (Fed. Cir. 1989). Accordingly, the Examiner is charged with the initial burden of identifying a source in the applied prior art for the requisite realistic motivation. *Smiths Industries Medical System v. Vital Signs, Inc.*, 183 F.3d 1347, 51 USPQ2d 1415 (Fed. Cir. 1999); *In re Mayne*, 104 F.3d 1339, 41

USPQ2d 1449 (Fed. Cir. 1997). The Examiner has not met the burden of identifying a source in Minato for the required realistic motivation of modifying the method of Hayashi to obtain the claimed method.

The only disclosure of the claimed method of manufacturing an integrated semiconductor device is found in Applicants' disclosure. Though, the Examiner asserted that the claimed method would have been obvious, the teaching or suggestion to make a claimed combination and the reasonable expectation of success must both be found in the prior art, and not be based on Applicants' disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). Apparently, the Examiner has relied on impermissible hindsight reasoning in reaching the conclusion of obviousness.

Claims 17 and 18 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hayashi in view of Minato et al. and further in view of Yoshida (JP 6-312918). These rejections are traversed, and reconsideration and withdrawal thereof respectfully requested.

The Examiner acknowledged that Hayashi and Minato do not disclose the mesh implantation masks having dot-like openings. The Examiner asserted that Yoshida teaches mesh implantation or dot implantation masks and concluded that it would have been obvious to incorporate Yoshida's teaching to enable regions having different concentrations to be formed in a single process.

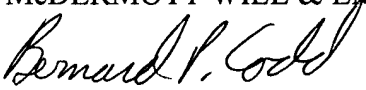
Hayashi, Minato, and Hayashi, whether taken alone or in combination, do not suggest the claimed method. Claims 17 and 18 are allowable for at least the same reasons as claim 13, as Yoshida does not cure the above-noted deficiencies Hayashi and Minato. In addition, Yoshida does not disclose the dot implantation mask, as required by claim 18.

In view of the above remarks, Applicants submit that this amendment should be entered, the application allowed and the case passed to issue. If there are any questions regarding these remarks or the application in general, a telephone call to the undersigned would be appreciated to expedite the prosecution of the application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP



Bernard P. Codd
Registration No. 46,429

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 BPC:MWE
Facsimile: 202.756.8087
Date: September 29, 2005

Please recognize our Customer No. 20277 as our correspondence address.